California State University, Fullerton

Computer Engineering

**EGCP 446 – Advanced Digital Design using Verilog HDL**

**(Fall 2019)**

**Project B: Unsymmetrical Character Display**

1. **Lab Description**

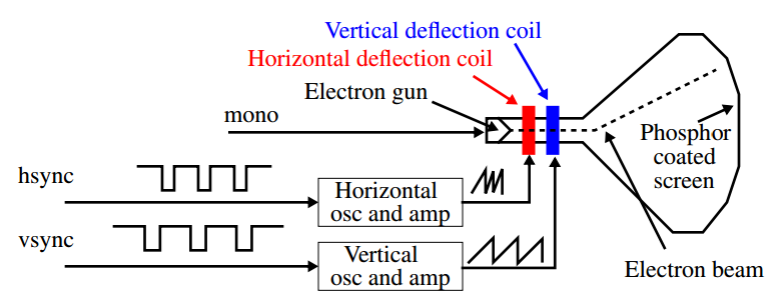
The Spartan 3 board uses 10 FPGA signals to create 8-bit color and two standard sync signals (HS-Horizontal Sync, and VS- sync).





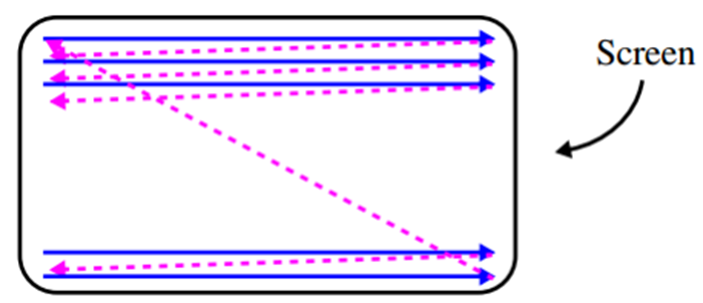
Here we consider an 8 color 640-480 pixel resolution interface for the older monochrome CRT model. The electron gun generates a focused electron beam that strikes the phosphor screen. The intensity of the electron beam and the brightness of the dot are determine by the voltage level of the external video input signal (mono signal). The mono signal is an analog signal whose voltage level is between 0 and 0.7 V.

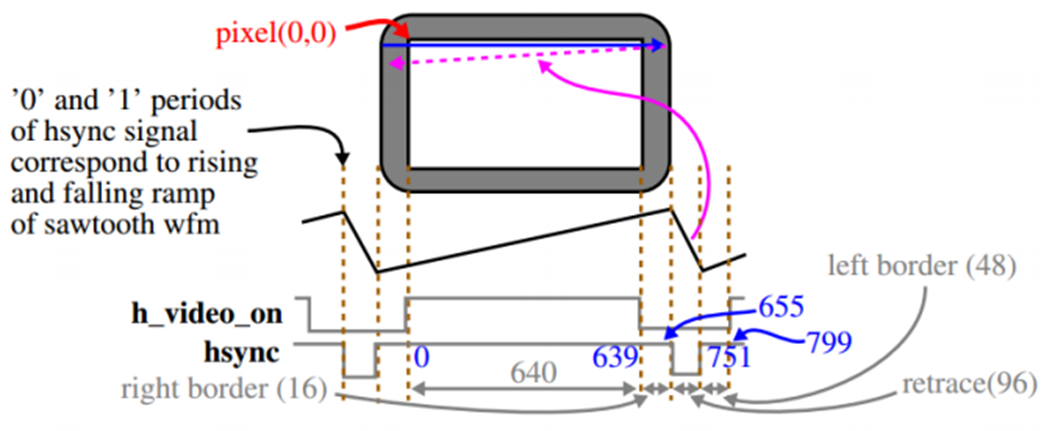
The horizontal and vertical deflection coils produce magnetic fields guide the electron beam to points on the screen.



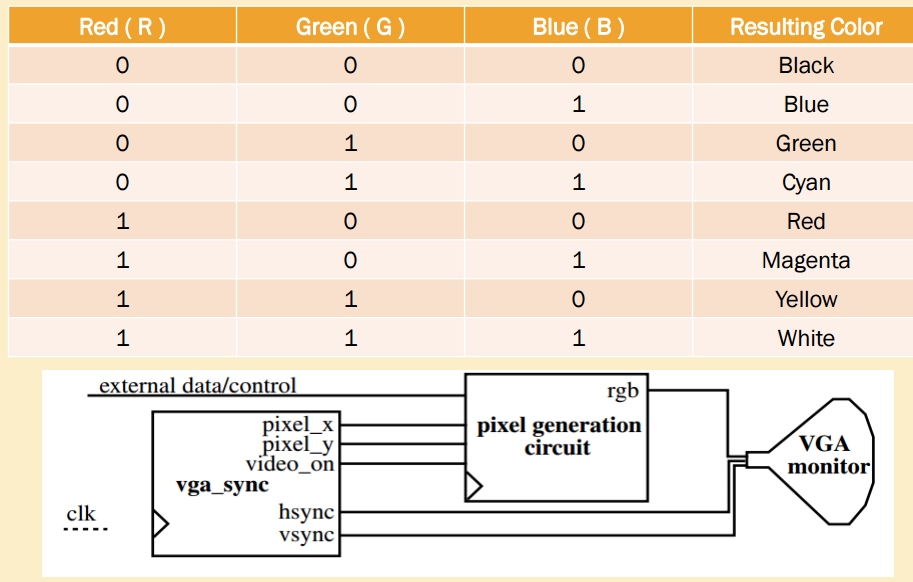
A color CRT is similar except that it has three electron beams, that are projected to the red, green and blue phosphor dots on the screen. The three dots are combined to form a pixel. The three voltage levels determine the intensity of each and therefore the color. The VGA port has five active signals, hsync, vsync, and three video signals for the red, green and blue beams. They are connected to a 15-pin D-subminiature connector.

The video signals are analog signals -- the video controller uses a D-to-A converter to convert the digital output to the appropriate analog level. If video is represented by an N-bit word, it can be converted to 2 𝑁analog levels. Three video signals can generate 2 3𝑁 different colors (called 3N-bit color). If 1-bit is used for each video signal, we get 2 3or 8 colors. If all three video signals are driven from the same 1-bit word, we get black & white.





**Video Controller:**



**Lab No 7 – Task**

* Create a group of four students. Please note this group can’t be change until the end of the semester.
* Create a LabProjB project and import all the provided Verilog files as well as the provided constraints file.
* Create Verilog files similar to Zero.v and One.v for displaying number two, three, four, five, six, seven, eight and nine.
* Modify the Pong\_graph\_st.v to display zero, one, two, three, four, five, six, seven, eight and nine on the VGA screen.
* Add the four switches to the pong\_top\_an.v and pong\_graph\_animate.v to select one of 10 numbers
* Generate the bit stream and program the FPGA with your design.
* Verify that the hardware’s behavior works as expected.
* Submit all your Verilog code and constrain files. Also, include the picture of your VGA screen for all the ten numbers.
* Please include the names of each group members involved.

Submit your Verilog code here

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